Fabrication of 22 nm half-pitch silicon lines by single-exposure self-aligned spatial-frequency doubling

Alex K. Raub, Dong Li, Andrew Frauenglass, and S. R. J. Brueck
Center for High Technology Materials, University of New Mexico, 1313 Goddard SE, Albuquerque, New Mexico 87106

(Received 10 June 2007; accepted 1 October 2007; published 7 December 2007)

The relentless progression of semiconductor technology to smaller feature sizes will likely soon outstrip the theoretical linear system limits of today’s optical lithography tools (a half-pitch of λ/4n or 34 nm with a 193 nm wavelength source and water immersion). We demonstrate a self-aligned process involving only a single lithographic exposure followed by spatial-frequency doubling that results in a half-scaling of the original pattern and have achieved a 22 nm half-pitch pattern with 193 nm water immersion. A lithographic pitch of 89 nm was realized with a 193 nm ArF-excimer laser source and de-ionized-water immersion interferometric lithography. A self-aligned spatial-frequency doubling technique, taking advantage of the well-known anisotropic etching of silicon by KOH, was used to affect the frequency doubling. A protective layer (metal) was deposited parallel to the (110) direction of a (100) silicon wafer and the sample was immersed in an appropriate KOH solution, resulting in a series of 44.5 nm opening width V-grooves terminated in 57° (111) faces etched into the silicon through the mask openings. The metal mask was removed to expose the previously protected high-etch-rate (100) surface of the sample for a second KOH etch. This results in a pattern at twice the original spatial frequency. A frequency-doubled pitch of 44.5 nm was achieved. An alternate, manufacturing-friendly, processing scheme related to standard gate sidewall passivation is proposed. © 2007 American Vacuum Society.

[DOI: 10.1116/1.2801889]

I. INTRODUCTION

The semiconductor industry is currently using 193 nm immersion lithography in its continuing drive for smaller features. With the use of hyper-numerical-aperture (NA) immersion steppers (NA ~ 1.35) the industry will achieve 45 nm half-pitch (hp) feature sizes. The next generation requires 32 nm hp features. With a 193 nm source, this requires a lithography tool with a NA of ~1.9 or a minimum refractive index for the immersion fluid and resist material greater than 2.04; and the 22 nm hp node would require a NA of 2.76 corresponding to a refractive index of 2.97. This is a daunting prospect, so it is appropriate to investigate alternate approaches for reaching the 22 nm hp node.

Double patterning allows patterning features near half the resolution of the exposure tool by printing one pattern at twice the desired pitch with features at the desired final sizes, transferring that pattern into an underlying sacrificial hard mask (taking advantage of nonlinearities in the photoresist and pattern transfer steps), printing a second pattern again at twice the final pitch with features at the desired final sizes but interleaved between the first pattern features, and again transferring the second pattern into the same underlying sacrificial hard mask. The hard mask now has the desired pattern at the final pitch, which is twice that available in a conventional single exposure. This final pitch is beyond the linear system bandpass (diffraction) limits of the optical lithography tool and arises entirely as a result of the nonlinear response of the photoresist and the processing. The sacrificial hard mask is used to transfer the pattern to the layer of interest and is then removed. This technique involves increased cost as there are many processing steps involved including multiple passes through lithography tools, that will lower wafer throughput and device yields. There is also a stringent registration requirement for the alignment between the two patterning exposures, which will be more than two times more demanding than required for the traditional single-exposure approach (which already scales with the reduced linear dimensions).

Another approach being investigated is double exposure. This is similar to double patterning, but both exposures are written into the same photoresistive layer and there is no requirement to transfer the pattern to a sacrificial hard mask. Trim masks for phase shift exposures are an existing example of this approach as is double-dipole illumination, which uses two masks to deal with the smallest features in the orthogonal spatial directions. Both of these approaches are restricted to the linear system limits of optics outlined above. Recently, there has been interest in incorporating a nonlinear response into a thin-film topcoat over the photoresist, for example, a reversible contrast enhancement layer or absorbance modulation optical lithography. This would allow a double exposure to access the same pattern dimensions as the double patterning technique, but with fewer process steps, and more importantly an inherent registration advantage since the wafer would not have to be removed from the lithography tool between exposures. There would still need to be an alignment between the two pattern masks, which is

---

"Electronic mail: alex.raub@ehmt.unm.edu"
"Electronic mail: brueck@ehmt.unm.edu"
usually less critical than between wafers. While there are active research efforts in these directions, many fundamental advances need to be made before these approaches can address volume-manufacturing requirements.

Self-aligned spatial-frequency doubling is proposed here as an alternative approach to the 22 nm hp lithography node. This approach utilizes a single exposure at twice the desired final pitch with features at roughly twice the final size. To be relevant, this exposure should be near the resolution limit of the exposure tool. Then through a process sequence that takes advantage of strong process spatial nonlinearities, a final pattern is created at the desired pitch (half the printed pitch) with perfect alignment and with the required feature sizes. Since there is only one exposure, this technique does not require a critical interexposure alignment, and typically has fewer process steps than double patterning. There remains a stringent process control constraint on the lithographic patterning to ensure an equal linespace final pattern.

We have demonstrated this frequency doubling approach with 193 nm immersion lithography starting with an initial 45 nm hp pattern and doubling it to a 22 nm half-pitch, which is, to our knowledge, the smallest hp pattern ever produced using a 193 nm source. (Using high index fluids a 30 nm hp single-exposure process has been reported. Using a solid immersion lens, a 25 nm hp has been demonstrated.) Once this periodic subresolution pattern is created, a lithography tool at the initial resolution can be used to personalize the pattern for circuit applications. This concept has been dubbed "graph-paper lithography." The idea is to produce a grating across the whole die at the minimum desired feature pitch. A trim mask is then used to remove parts of the grating to form the final pattern. The trim mask does not require the same resolution as the graph paper and can be therefore printed using a lower resolution lithography tool. A schematic representation of graph-paper lithography is shown in Fig. 1.

II. EXPERIMENT

A proof of concept demonstration of a 22 nm half-pitch grating was made using a single-exposure self-aligned spatial-frequency doubling technique. To our knowledge, this is the smallest half-pitch structure demonstrated to date using 193 nm lithography. The initial pattern was made using 193 nm immersion lithography at a 45 nm half-pitch resist process. The final 22 nm half-pitch grating was etched into a silicon wafer.

A. Process

A maskless, interferometric lithography approach involving the interference of two coherent beams was used for the initial lithographic exposure and a pair of anisotropic KOH etching steps provided the frequency doubling. The result was 22 nm hp silicon lines, but the scaling factor is not limited to 2 and can, in principle, be increased further; additionally this concept is applicable at any scale, so that if higher index immersion fluids allow reaching the 32 nm hp node, self-aligned frequency doubling will permit patterning to a 16 nm hp and beyond.

The 89 nm lithographic pitch \( \lambda \) was achieved with a 193 nm ArF-excimer laser source and immersion interferometric lithography using prism coupling and de-ionized-water immersion. Figure 2 shows the 45 nm printed resist pattern on the silicon wafer. The 193 nm resist was \( \sim 85 \) nm thick on a dual-layer bottom antireflective coating (DLBARC) with a 32 nm bottom layer and a 45 nm upper layer to form a 77 nm BARC layer. The DL-BARC was sequentially patterned using an oxygen plasma etch process. A 10–20 nm thick Cr layer was deposited on the patterned silicon surface using an electron plasma etch evaporator. The Cr on top of the resist/BARC pattern was removed using an acetone bath lift-off process, followed by a piranha clean. The result is a Cr hard mask atop the silicon surface. Figure 3 shows the schematic process after the Cr metal lift-off. This technique takes advantage of the well-known anisotropic etching of silicon by KOH and other alkali metal hydroxides. KOH etches along the (100) crystal plane several hundred times faster than along the (111) plane of silicon. A self-terminating V-groove with (111) sidewalls results from etching of an exposed (100) region confined along the (110) directions. Thus the steps in the frequency doubling process are (1) definition of a Cr-mask layer by lithography and pattern transfer (lift-off for this experiment); (2) KOH etching of the width \( \lambda/2 \) Si areas to reveal V grooves with a sidewall dimension of \( \lambda/4 \); (3) removal of the Cr-mask layers; and (4) a second KOH etching producing an additional interleaved set of V-grooves. The second etching has only a small impact on the first set of V grooves as a result of the self-limiting of the KOH-etch process. The final result is a
frequency-doubled V-groove pattern at $\Lambda/2$. The critical pattern definition step, ensuring that both sets of V grooves have the same width, is controlled by the line:space ratio of the lithographic exposure.

B. Results

As is seen in Fig. 4 the grating period is 44.5 nm with 22 nm hp lines. There is an alternation in the gap width (wide narrow) that shows that the original patterning (lithography and metal lift-off) did not quite meet the requirements for a uniform final pitch. The roughness in the pattern is induced by the imperfections in pattern definition and transfer at these very small scales. For larger scale (and deeper) patterns, the anisotropy of the KOH etching typically eliminates much of this process-induced roughness; the roughness reveals high-etch rate planes which are removed by further etching finally stopping on the lowest etch rate (111) planes. The fact that the KOH etch was unable to smooth out the line-edge roughness and form well-defined (111) faceted grooves at 22 nm hp dimensions suggests that there is some surface damage from the wafer polishing that disrupts the crystal structure and stops the etch process. Reclaimed wafers were used for this experiment, which may account for an increased level of surface damage; more detailed analysis and experiments are necessary to fully elucidate these effects. Figure 5 shows a micrograph of an area of the structure that includes several defects in the original lithographic pattern. V grooves are evident at widths of $\Lambda/2$, $\Lambda$, and $2\Lambda$. When examining facets at a defect where one line is missing, the $\Lambda$ wide V groove is further defined and clearly smoother than the 22 nm hp $\Lambda/2$ wide V grooves. At scale several times larger than the 22 nm hp pattern in Fig. 5, the facets of the wider and deeper KOH etched structures appear significantly smoother and clearly reveal (111) crystallographic orientations. The tops of all of the V grooves still retain comparable roughness to the $\Lambda/2$ wide 22 nm hp features, providing some insight into the mechanisms responsible for the roughness.

![Fig. 5. SEM of a region near a defect in the lithographic pattern. Note the smooth sidewalls of the larger KOH-etched V grooves along with a comparable roughness of the top layers for all three observed V-groove dimensions.](image)

![Fig. 6. Schematic process flow for an alternative, manufacturing-friendly, self-aligned frequency-doubling scheme similar to traditional gate sidewall passivation processes.](image)
III. ALTERNATE MANUFACTURING-FRIENDLY FREQUENCY DOUBLING TECHNIQUE

This proof-of-principle experiment resulted in exposing (111) facets on a (100) silicon wafer. This is not desirable for semiconductor manufacturing because of the topography and because of the high oxide leakage current densities for a (111) surface. A manufacturing-friendly alternate approach to single-exposure self-aligned spatial-frequency doubling technique uses polysilicon with oxide spaces atop a standard (100) wafer, as illustrated in Fig. 6. The process uses a poly-silicon film on a nitride or other hard-mask material. The polysilicon is patterned through standard lithography techniques at twice the final pitch, using the hard mask as an etch stop. An oxide is then either grown or conformally deposited on the silicon lines at the thickness of the desired line size. The oxide is then etched back to form a spacer around the polysilicon lines and the polysilicon is removed, leaving the oxide lines atop the hard mask. The oxide lines serve as a mask for etching the continuous hard-mask film, which is then used to transfer the final spatial-frequency-doubled pattern to the desired underlying layers. There are many other process sequences that produce frequency-doubled patterns. Related process sequences have been implemented for the formation of sidewall spacers or to affect sidewall passivation. Additional work is necessary to assess the suitability of these process sequences for volume-manufacturing applications.

IV. SUMMARY

A single-exposure self-aligned spatial-frequency doubling technique has been demonstrated with a record 22 nm hp structure, well beyond the linear system limit of water immersion optical lithography using a 193 nm source. By using a single-exposure self-aligned spatial-frequency doubling technique to print a uniform, large-area grating and using a trim mask to create a final microchip device structure, it is possible to use graph-paper lithography to achieve a 32 or 22 nm hp lithographic pattern using a 193 nm immersion lithography tool designed for the 45 nm hp lithography node.

2G. Cooper, EIPBN’07 (unpublished), Paper No. 2A.1.